CLMPTO 09/28/04 JW

Cancel Claims 91-98, 136-148,154

99. (Previously Amended): A method for automatically constructing a routing tag for a cell based on an address provided by a bus operation on a bus connected to a first node of a system interconnect comprising the steps of:

capturing said address from said bus;

converting said address into a value stored in said routing tag;

detecting an interrupt condition change at said first node, said interrupt condition change comprising either an interrupt assertion or an interrupt deassertion;

creating an interrupt cell at said first node responsive to the detecting said interrupt condition change, said interrupt cell addressed to a second node and containing said interrupt condition change;

transporting said interrupt cell to said second node; and

asserting an interrupt signal at said second node responsive to said interrupt condition change.

100. (Previously Presented): The method of claim 99 wherein the step of asserting further comprises steps of:

recognizing said interrupt cell containing said interrupt assertion at said second node; and

incrementing an up/down counter.

101. (Previously Presented): The method of claim 100 wherein the step of asserting further comprises steps of:

detecting that said up/down counter is non-zero; and

posting an interrupt at said second node.

102. (Previously Presented): The method of claim 99 wherein said cell further comprises a first node identifier and the step of asserting further comprises:

saving said first node identifier and said interrupt condition change.

103. (Previously Presented): The method of claim 99 wherein the step of asserting further comprises steps of:

recognizing said interrupt cell containing said interrupt deassertion; and

decrementing an up/down counter.

104. (Previously Presented): The method of claim 103 wherein the step of asserting further comprises steps of:

detecting that said up/down counter is zero; and

clearing an interrupt at said second node.

104. (Previously Presented): The method of claim 99 wherein said interrupt cell comprises an interrupt security code and the step of asserting further comprises matching said interrupt security code with a second node interrupt security code.

105. (Previously Presented): The method of claim 99 wherein said interrupt condition is a result of a bus error on said bus.

107. (Previously Presented): The method of claim 105 wherein said bus is PCI bus and said bus error results in a SERR assertion.

Claims 108-121 (Canceled).

122. (Previously Presented): A method for automatically constructing a routing tag for a cell based on an address provided by a bus operation on a bus connected to a first node of a system interconnect comprising the steps of:

capturing said address from said bus;

converting said address into a value stored in said routing tag;

converting said bus operation into said cell;

transporting said cell over said system interconnect from said first node to a second node; and

performing an equivalent bus operation on a second computer system bus by said second node after receipt of said cell by said second node.

123. (Previously Presented): The method of claim 122 wherein said first bus is a first PCI bus and said second bus is a second PCI bus.

124. (Previously Presented): The method of claim 122 wherein said first bus is a PCI bus and said second bus is not.

126. (Previously Presented): The method of claim 123 further comprising steps of:

asserting a second cell containing status of said equivalent bus operation;

transporting said second cell to said first node;

completing said bus operation upon receipt of said second cell.

131. (Previously Presented): The method of claim 122 wherein the step of converting includes steps of:

determining, responsive to said bus operation, an identifier for said second node from an address mapping content addressable memory (ADDCAM); and

including said identifier in said cell.

127. (Previously Amended): An apparatus for successfully constructing a routing tag for a cell based on an address provided by a host operation on a bus connected to a first node of a system interconnect comprising:

an address capturing mechanism configured to capture said address from said bus;

an address conversion mechanism configured to convert said address from said bus into a value stored in said routing tag of said cell;

an interrupt detection mechanism configured to detect an interrupt condition change at said first node, said interrupt condition change comprising either an interrupt assertion or an interrupt deassertion;

an interrupt cell creation mechanism configured to create an interrupt cell at said first node responsive to the interrupt detection mechanism, said interrupt cell being addressed to a second node and containing said interrupt condition change;

A cell transportation mechanism configured to transport said interrupt cell to said second node; and

an interrupt servicing mechanism configured to assert an interrupt signal at said second node responsive to said interrupt condition change.

128. (Previously Presented): The apparatus of claim 127 wherein the interrupt assertion mechanism further comprises:

an interrupt assertion recognition mechanism at said second node configured to recognize said interrupt cell containing said interrupt assertion and transmit an up/down notice.

129. (Previously Presented): The apparatus of claim 128 wherein the interrupt assertion mechanism further comprises:

a pool interrupt mechanism configured to detect that said up/down notice is non-zero and to post an interrupt at said second node.

130. (Previously Presented): The apparatus of claim 127 wherein said cell further comprises a first node identifier and the interrupt assertion mechanism further comprises:

a storage mechanism configured to save said first node identifier and said interrupt condition change.

131. (Previously Presented): The apparatus of claim 127 wherein the interrupt assertion mechanism further comprises:

an interrupt deassertion recognition mechanism at said second node configured to recognize said interrupt cell containing said interrupt deassertion, and decrement an up/down counter.

132. (Previously Presented): The apparatus of claim 130 wherein the interrupt assertion mechanism further comprises:

a clear interrupt mechanism configured to detect that said upstream source is done and to clear an interrupt at said second node.

139. (Previously Presented): The apparatus of claim 137 wherein said interrupt will comprises an interrupt security code and the interrupt insertion mechanism further comprises:

an interrupt security mechanism configured to match said interrupt security code with a second node interrupt security code.

134. (Previously Presented): The apparatus of claim 139 wherein said interrupt condition is a result of a bus error on said bus.

135. (Previously Presented): The apparatus of claim 134 wherein said bus is a PCI bus and said bus error result in a SERR assertion.

Claims 136-148 (Canceled).

149. (Previously Amended): An apparatus for automatically connecting a routing tag for a cell based on an address provided by a bus operation on a bus connected to a first node of a system interconnect computing:

an address capturing mechanism configured to capture said address from said bus;

an address association mechanism configured to convert said address from said bus into a value stored in said routing tag of said cell;

a first cell generation mechanism of said first node configured to convert said bus operation into said cell;

a first cell transportation mechanism configured to transport said cell over said system interconnect from said first node to a second node; and

a bus operation mechanism of said second node configured to perform an equivalent bus operation on a second computer system bus after receipt of said cell by said second node.

150. (Previously Presented): The apparatus of claim 149 wherein the first cell generation mechanism further comprises:

an address mapping content addressable memory (AMCAM) responsive to said bus operation to output a an identifier for said first node; and

a cell address mechanism configured to include said identifier in said cell.

151. (Previously Presented): The apparatus of claim 149 wherein said first bus is a first PCI bus and said second bus is a second PCI bus.

152. (Previously Presented): The apparatus of claim 149 wherein said first bus is a PCI bus and said second bus is not.

151. (Previously Presented): The apparatus of claim 149 further comprising:

a result acquisition mechanism in said second node configured to obtain a result from performance of said equivalent bus operation on said second bus;

a second cell generation mechanism at said second node configured to convert said result into a second cell;

a second cell transportation mechanism at said second node configured to transmit said second cell over said system interconnect from said second node to said first node; and

a bus operation completion mechanism at said first node configured to complete said bus operation on receipt of said second cell.

154. (Canceled).